genapta

GEN-1130-5

Counter/Shift Register Interface IC

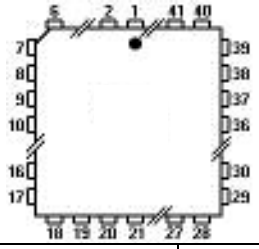
V2.0-071204

Features

- **Digital Input Filter**
- **30 bit Up/Down counter**
- **30 bit PISO Shift Register**
- **Zero Reference mark support**
- **Counter Inhibit**
- **Tristate bus output**
- **High Performance - Maximum input speed of 10MHz**
- **5V or 3.3V I/O Capability**
- **Samples are available**

Description

The GEN-1130-5 is a high-performance multi-purpose Interface IC. It contains a digital input filter connected to a resettable 30-bit up/down counter and PISO shift register, allowing consistent extraction of the counter value with low interface pin counts.



Package: 44 Pin PLCC
Operating Temperature Range: -20ºC to 85ºC

Parameters:

Parameter	Min	Max	Units
V_{CCINT} Supply voltage for internal logic	4.75	5.25	V
V_{CCIO} Supply voltage for output drivers	4.75 3.0	5.25 3.6	V
Low level input voltage	0	0.8	V
High level input voltage	2.0	V_{CCINT}+0.5	V
Output Voltage	0	V_{CCIO}	V

Parameter	Test Conditions	Min	Max	Units
Output high voltage for 5V outputs	I= –4.0mA V_{CC}= Min	2.4		V
Output high voltage for 3.3V outputs	I= –3.2mA V_{CC}= Min	2.4		V
Output low voltage for 5V outputs	I= 24mA V_{CC}= Min		0.5	V
Output low voltage for 3.3V outputs	I= 10mA V_{CC}= Min		0.4	V
Input leakage current	V_{CC}= Max V_{IN}= GND or V_{CC}		±10	µA
I/O high-Z leakage current	V_{CC}= Max V_{IN}= GND or V_{CC}		±10	µA
I/O capacitance	V_{IN}= GND f= 1.0MHz		10	pF

Important Notice

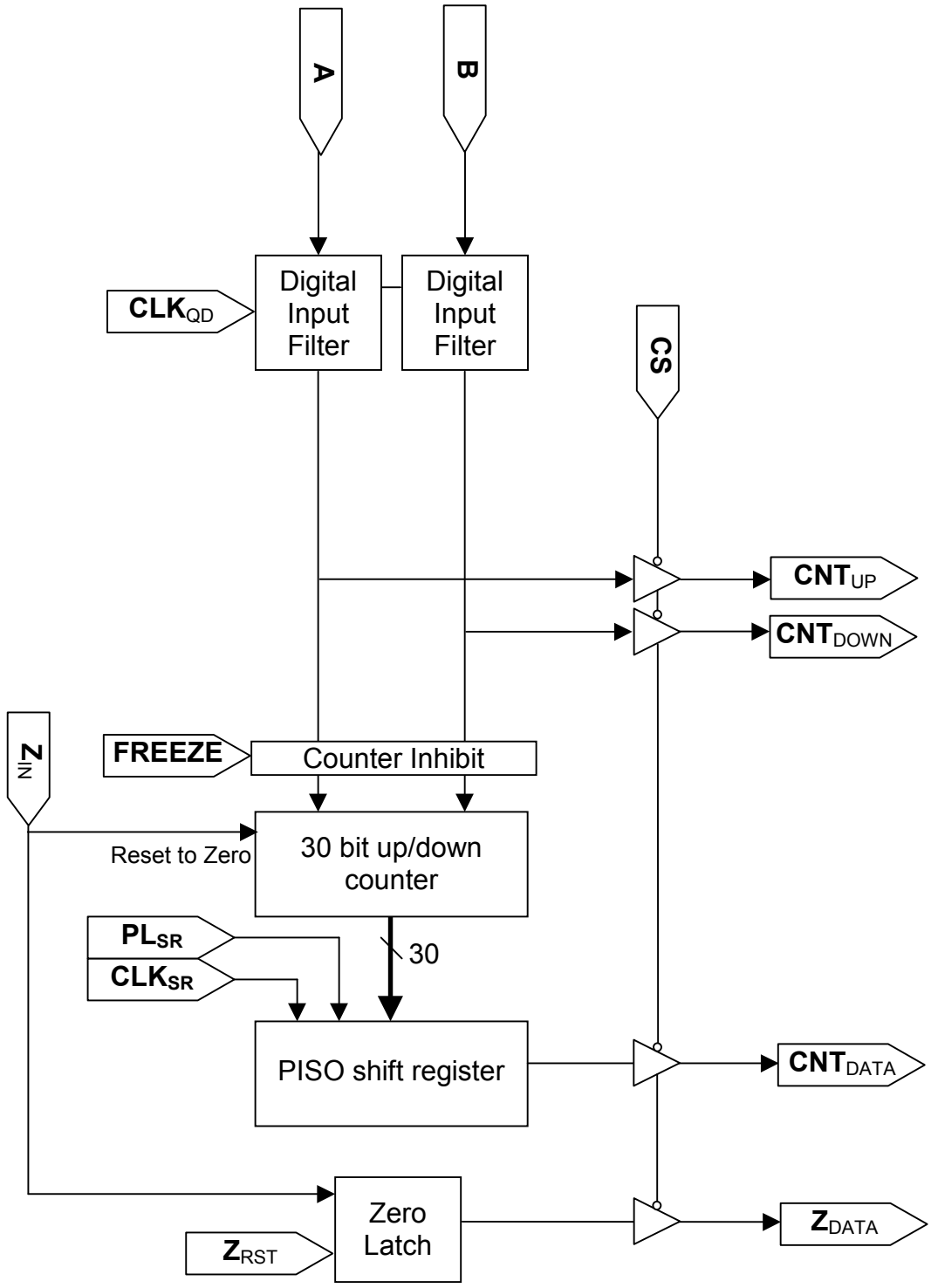
genapta decoders are not recommended for use in safety critical applications. eg: Life support systems, critical care medical equipment, ABS braking systems and power steering. Please contact us for clarification if required

Pin Assignments*

Pin	I/O	Name	Description
2	I	PL_{SR}	Shift Register Parallel Load
5	I	CLK_{QD}	Input from external clock source (max 32MHz). Determines maximum input speed for Quadrature Decoder and Input Filter.
6	I	CLK_{SR}	Shift Register Clock
7	I	Z_{RST}	Zero reset. Rising edge turns Z_{DATA} low. Z_{RST} is asynchronous with respect to any other input signal.
9	O	Z_{DATA}	Zero data. Initially low, will go high on rising edge of Z_{IN}, and remain high until a rising edge on $Z_{RST.}$
10	-	GND	GND
11	O	CNT_{DATA}	Count Data. Output from Shift Register
21	-	V_{CCINT}	+5V
23	-	GND	GND
31	-	GND	GND
32	-	V_{CCIO}	+5V/+3.3V - I/O Voltage
35	I	A	Count up. A rising edge on A increments the counter by 1.
36	O	CNT_{UP}	Count up. Connected to the output of the digital input filter.
37	I	B	Count down. A rising edge on B decrements the counter by 1.
38	I	$\overline{FREEZE}$	Inhibit any counter value change when high. Normal operation when low.
39	I	Z_{IN} (RST)	Zero/Reference mark input. Reset internal position counter to 0. Sets $Z_{DATA.}$ Z_{IN} is asynchronous with respect to any other input signal.
40	I	$\overline{CS}$	Chip Select, when high, CNT_{DATA}, CNT_{UP}, CNT_{DOWN} and Z_{DATA} are undriven (tristate), when low, the pins drive their respective values.
41	-	V_{CCINT}	+5V
43	O	CNT_{DOWN}	Count down. Connected to the output of the digital input filter.

***All other package pins should be tied to GND to ensure correct operation.**

Functional Block Diagram:



Component Description

Digital Input Filter

The optional digital input filter is responsible for removing noise from the incoming quadrature signals. A delay filter of 3 CLK_{QD} cycles rejects spikes of short duration. The input data is tested for a stable level being present for 3 consecutive rising clock edges, and the filtered output will only change after the input signal has remained consistent for this time. Short noise spikes and pulses shorter than 2 clock periods are ignored.

The operation of the digital input filter places constraints on the maximum speed of input signals A and B. Because the signals must remain constant for 3 clock cycles, they can have an absolute maximum frequency of (CLK_{QD} / 3), and should be slower than this where noise is present. It is recommended that the input frequency is less than CLK_{QD} / 6.

Counter

This consists of a 30 bit binary up/down counter which counts on rising edges of the A and B inputs.

When FREEZE is high, the counter's value will not change.

The counter can be cleared to 0 asynchronously by a rising edge on Z_{IN}.

Shift Register

The Shift Register operates on a separate clock to the rest of the components.

Data is latched into the shift register on a rising edge of CLK_{SR} while PL_{SR} is held high. All 30 bits of data are transferred simultaneously.

The LSB of the counter's value is then available immediately on CNT_{DATA}.
On each further rising edge of CLK_{SR} (with PL_{SR} low) the next highest bit of the counter's value is latched to CNT_{DATA}.
After 29 CLK_{SR} rising edges, further CLK_{SR} rising edges will latch 0 to CNT_{DATA}.

At any point if PL_{SR} is held high for one rising edge of CLK_{SR} then a new count value will be latched into the shift register.

Zero/ Reference Mark

A rising edge on Z_{IN} will:
- Set the counter to have value 0
- Latch Z_{DATA} high.

Z_{DATA} will then remain high until a rising edge occurs on Z_{RESET}, which will latch Z_{DATA} low again.

If a rising edge occurs on $Z_{IN,}$ while Z_{RESET} is high, then Z_{DATA} will still become latched high.

Z_{IN} and Z_{RESET} are asynchronous input signals.

While FREEZE is high, the counter's value will be inhibited from changing.

Tristate Output

All chip outputs are tristate-capable, to permit easy connection to a bus. When CS is high, all outputs become undriven. When CS is low, outputs drive their respective values.