genapta

# GEN-2122-5

# Quadrature Decoder/Counter/Shift Register Interface IC

**V2.0-071204**

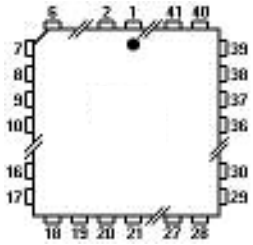
## Features

- **Digital Input Filter**
- **Quadrature Decoder**
- **22 bit Up/Down counter**
- **22 bit PISO Shift Register**
- **Zero Reference mark support**
- **Counter Inhibit**
- **Tristate bus output**
- **High Performance - Maximum input speed of 10MHz**
- **5V or 3.3V I/O Capability**
- **Samples are available**

**Package:** 44 Pin PLCC
**Operating Temperature Range:** -20ºC to 85ºC

## Description

The GEN-2122-5 is a high-performance multi-purpose Interface IC. It contains a digital input filter and quadrature decoder with exposed outputs. This is also connected to a resettable 22-bit up/down counter and PISO shift register, allowing consistent extraction of the counter value with low interface pin counts.




**Parameters:**

| Parameter | Min | Max | Units |
|---|---|---|---|
| $V_{CCINT}$ Supply voltage for internal logic | 4.75 | 5.25 | V |
| $V_{CCIO}$ Supply voltage for output drivers | 4.75<br>3.0 | 5.25<br>3.6 | V |
| Low level input voltage | 0 | 0.8 | V |
| High level input voltage | 2.0 | $V_{CCINT}$+0.5 | V |
| Output Voltage | 0 | $V_{CCIO}$ | V |

| Parameter | Test Conditions | Min | Max | Units |
|---|---|---|---|---|
| Output high voltage for 5V outputs | I= –4.0mA $V_{CC}$= Min | 2.4 | | V |
| Output high voltage for 3.3V outputs | I= –3.2mA $V_{CC}$= Min | 2.4 | | V |
| Output low voltage for 5V outputs | I= 24mA $V_{CC}$= Min | | 0.5 | V |
| Output low voltage for 3.3V outputs | I= 10mA $V_{CC}$= Min | | 0.4 | V |
| Input leakage current | $V_{CC}$= Max<br>$V_{IN}$= GND or $V_{CC}$ | | ±10 | µA |
| I/O high-Z leakage current | $V_{CC}$= Max<br>$V_{IN}$= GND or $V_{CC}$ | | ±10 | µA |
| I/O capacitance | $V_{IN}$= GND f= 1.0MHz | | 10 | pF |

## Important Notice

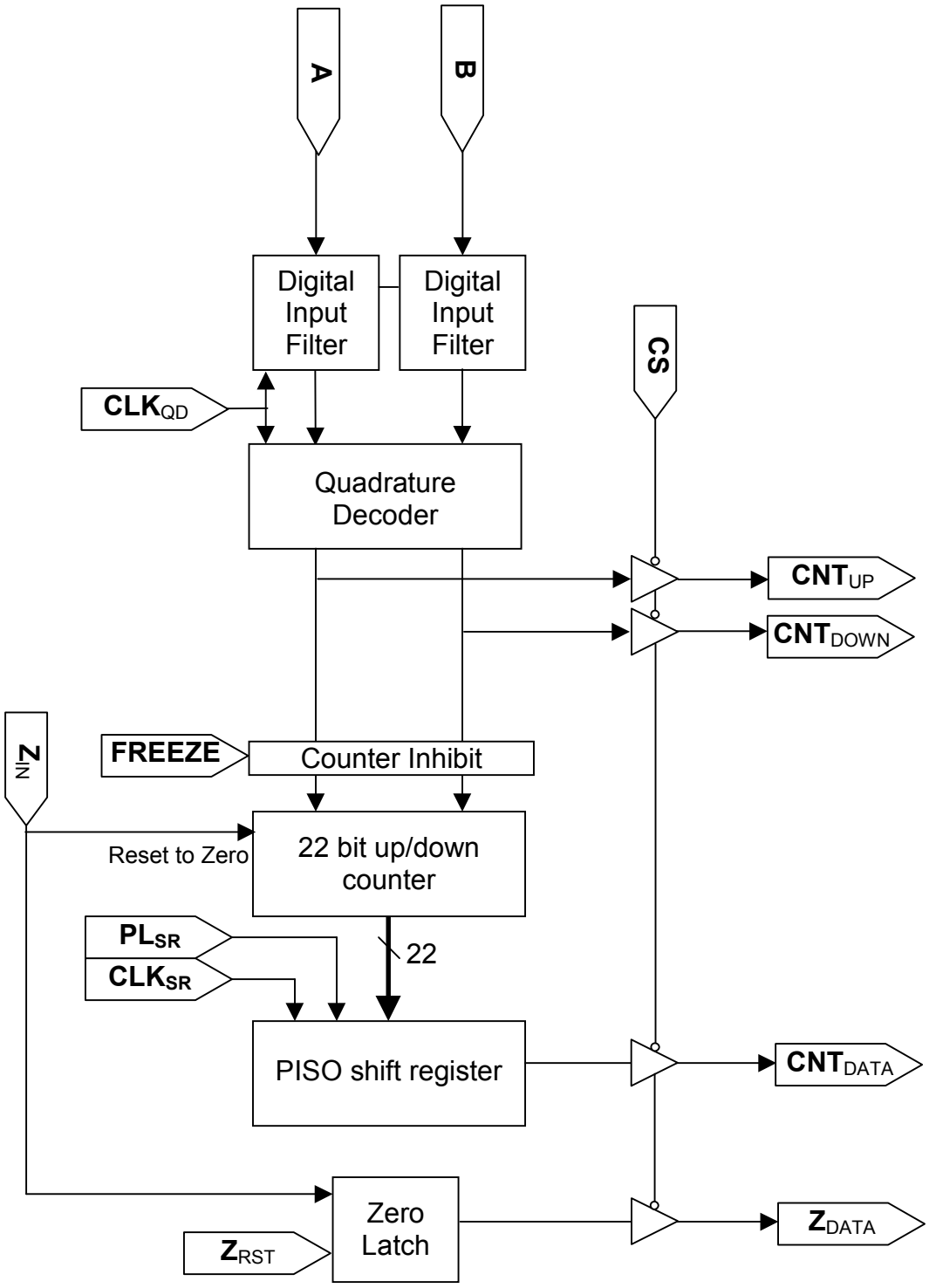
genapta decoders are not recommended for use in safety critical applications. eg: Life support systems, critical care medical equipment, ABS braking systems and power steering. Please contact us for clarification if required.

## Pin Assignments*

| Pin | I/O | Name | Description |
|---|---|---|---|
| **2** | I | $PL_{SR}$ | Shift Register Parallel Load |
| **5** | I | $CLK_{QD}$ | Input from external clock source (max 32MHz). Determines maximum input speed for Quadrature Decoder and Input Filter. |
| **6** | I | $CLK_{SR}$ | Shift Register Clock |
| **7** | I | $Z_{RST}$ | Zero reset. Rising edge turns $Z_{DATA}$ low. $Z_{RST}$ is asynchronous with respect to any other input signal. |
| **9** | O | $Z_{DATA}$ | Zero data. Initially low, will go high on rising edge of $Z_{IN}$, and remain high until a rising edge on $Z_{RST.}$ |
| **10** | - | GND | GND |
| **11** | O | $CNT_{DATA}$ | Count Data. Output from Shift Register |
| **21** | - | $V_{CCINT}$ | +5V |
| **23** | - | GND | GND |
| **31** | - | GND | GND |
| **32** | - | $V_{CCIO}$ | +5V/+3.3V - I/O Voltage |
| **35** | I | A | Quadrature input A<br>A and B (pin 37) accept outputs from a quadrature encoded source, eg optical encoder. A and B are nominally +/- 90 degrees out of phase. |
| **36** | O | $CNT_{UP}$ | Count up. Will pulse high for one clock cycle whenever the quadrature decoder detects a upwards movement. |
| **37** | I | B | Quadrature input B (see pin 35) |
| **38** | I | $\overline{\text{FREEZE}}$ | Inhibit any counter value change when high. Normal operation when low. |
| **39** | I | $Z_{IN}$ (RST) | Zero/Reference mark input. Reset internal position counter to 0. Sets $Z_{DATA.}$ $Z_{IN}$ is asynchronous with respect to any other input signal. |
| **40** | I | $\overline{\text{CS}}$ | Chip Select, when high, $CNT_{DATA}$, $CNT_{UP}$, $CNT_{DOWN}$ and $Z_{DATA}$ are undriven (tristate), when low, the pins drive their respective values. |
| **41** | - | $V_{CCINT}$ | +5V |
| **43** | O | $CNT_{DOWN}$ | Count down. Will pulse high for one clock cycle whenever the quadrature decoder detects a downwards movement. |

***All other package pins should be tied to GND to ensure correct operation.**

## Functional Block Diagram:



# Component Description

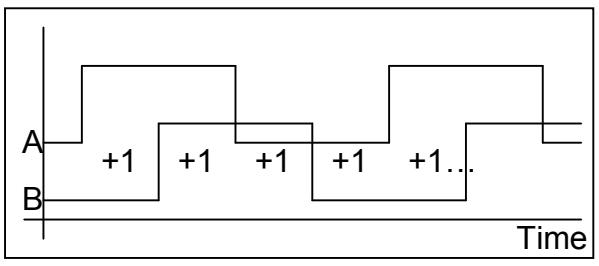
## Digital Input Filter

The digital input filter is responsible for removing noise from the incoming quadrature signals. A delay filter of 3 clock cycles rejects spikes of short duration. The input data is tested for a stable level being present for 3, and the filtered output will only change after the input signal has remained consistent for this time. Short noise spikes and pulses shorter than 2 clock periods are ignored.

The operation of the digital input filter places constraints on the maximum speed of input signals A and B. Because the signals must remain constant for 3 clock cycles, they can have an absolute maximum frequency of ($CLK_{QD}$ / 3), and should be slower than this where noise is present. It is recommended that the input frequency is less than $CLK_{QD}$ / 6.

## Quadrature Decoder

The quadrature decoder decodes the filtered signals into count information. A 4X quadrature decoder is implemented, and the counter will increase or decrease by one for each signal transition. (see inset diagram)




The decoder samples the filtered A and B signals, and calculates the up/down transition based on current and past state. When a transition is detected, either $CNT_{UP}$ or $CNT_{DOWN}$ will go high for one clock cycle. These pulses also form inputs to the internal counter.

Input line A leading line B results in counting up. Line B leading line A results in counting down.

Illegal state transitions (both signals changing between two $CLK_{QD}$ rising edges) will cause the count to remain constant.

## Counter

This consists of a 22-bit binary up/down counter which counts on rising edges of the pulses output from the quadrature decoder.

When FREEZE is high, the counter's value will not change.

All 22 bits of data are passed in parallel to the shift register.

The counter is cleared to 0 asynchronously by a rising edge on $Z_{IN.}$

## Shift Register

The Shift Register operates on a separate clock to the rest of the components.

Data is latched into the shift register on a rising edge of $CLK_{SR}$ while $PL_{SR}$ is held high.

The LSB of the counter's value is then available immediately on $CNT_{DATA}$.

On each further rising edge of $CLK_{SR}$ (with $PL_{SR}$ low) the next highest bit of the counter's value is latched to $CNT_{DATA.}$

After 21 $CLK_{SR}$ rising edges, further $CLK_{SR}$ rising edges will latch 0 to $CNT_{DATA}$.

At any point if $PL_{SR}$ is held high for one rising edge of $CLK_{SR}$ then a new count value will be latched into the shift register.

## Zero/ Reference Mark

A rising edge on $Z_{IN}$ will:

- Set the counter to have value 0
- Latch $Z_{DATA}$ high.

$Z_{DATA}$ will then remain high until a rising edge occurs on $Z_{RESET}$, which will latch $Z_{DATA}$ low again.

If a rising edge occurs on $Z_{IN,}$ while $Z_{RESET}$ is high, then $Z_{DATA}$ will still become latched high.

$Z_{IN}$ and $Z_{RESET}$ are asynchronous input signals.

While FREEZE is high, the counter's value will be inhibited from changing.

## Tristate Output

All chip outputs are tristate-capable, to permit easy connection to a bus. When CS is high, all outputs become undriven. When CS is low, outputs drive their respective values.