genapta

GEN-2212-5

Dual Channel Quadrature Decoder/Counter/Shift Register Interface IC

V2.0-071204

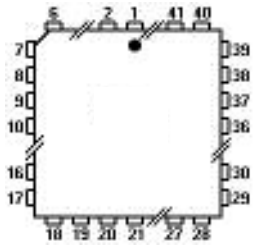
Features

- **Simultaneous dual quadrature decoders with dual 12 bit Up/Down counter**
- **2 pulse Digital Input Filter**
- **12 bit PISO Shift Register**
- **Zero reference mark support**
- **Tristate bus output**
- **High Performance - Maximum input speed of 15MHz**
- **5V or 3.3V I/O Capability**
- **Samples are available**

Package: 44 Pin PLCC
Operating Temperature Range: -20ºC to 85ºC

Description

The GEN-2212-5 is a high-performance dual channel encoder Interface IC. Both channels have digital input filters, high-speed quadrature decoders with exposed outputs. Each channel has a 12-bit up/down counter connected to a shared PISO shift register, allowing consistent extraction of the counter value with low interface pin counts.



Parameters:

Parameter	Min	Max	Units
V_{CCINT} Supply voltage for internal logic	4.75	5.25	V
V_{CCIO} Supply voltage for output drivers	4.75 3.0	5.25 3.6	V
Low level input voltage	0	0.8	V
High level input voltage	2.0	V_{CCINT}+0.5	V
Output Voltage	0	V_{CCIO}	V

Parameter	Test Conditions	Min	Max	Units
Output high voltage for 5V outputs	I= –4.0mA V_{CC}= Min	2.4		V
Output high voltage for 3.3V outputs	I= –3.2mA V_{CC}= Min	2.4		V
Output low voltage for 5V outputs	I= 24mA V_{CC}= Min		0.5	V
Output low voltage for 3.3V outputs	I= 10mA V_{CC}= Min		0.4	V
Input leakage current	V_{CC}= Max V_{IN}= GND or V_{CC}		±10	µA
I/O high-Z leakage current	V_{CC}= Max V_{IN}= GND or V_{CC}		±10	µA
I/O capacitance	V_{IN}= GND f= 1.0MHz		10	pF

Important Notice

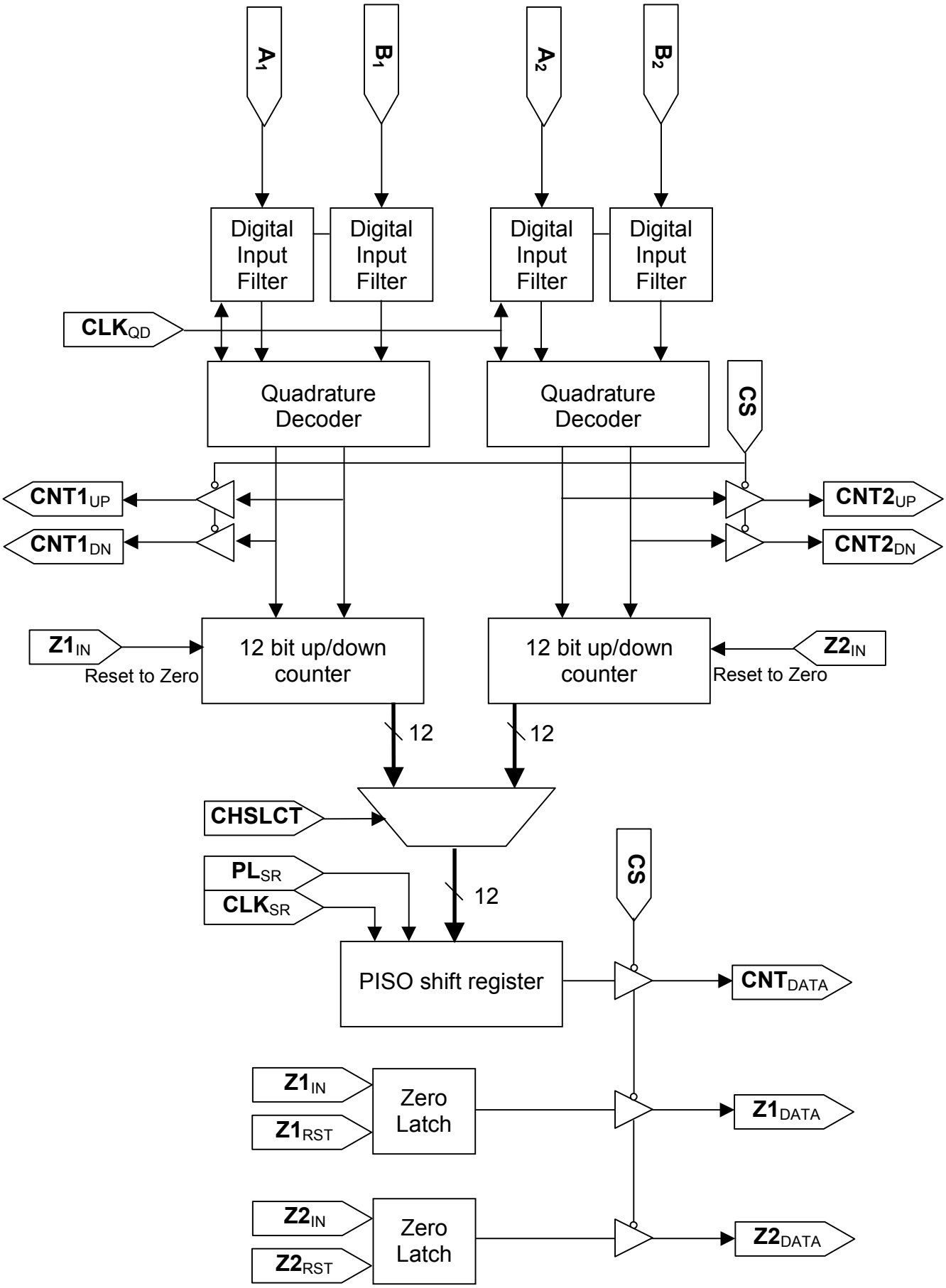
genapta decoders are not recommended for use in safety critical applications. eg: Life support systems, critical care medical equipment, ABS braking systems and power steering. Please contact us for clarification if required.

Pin Assignments*

Pin	I/O	Name	Description
2	I	PL_{SR}	Shift Register Parallel Load
5	I	CLK_{QD}	Input from external clock source (max 32MHz). Determines maximum input speed for Quadrature Decoder and Input Filter.
6	I	CLK_{SR}	Shift Register Clock
7	I	$Z1_{RST}$	Channel 1 Zero reset. Rising edge turns $Z1_{DATA}$ low. $Z1_{RST}$ is asynchronous with respect to any other input signal.
8	I	$Z2_{RST}$	Channel 2 Zero reset. Rising edge turns $Z2_{DATA}$ low. $Z2_{RST}$ is asynchronous with respect to any other input signal
9	O	$Z1_{DATA}$	Channel 1 Zero data. Initially low, will go high on rising edge of $Z1_{IN}$, and remain high until a rising edge on $Z1_{RST.}$
10	-	GND	GND
11	O	CNT_{DATA}	Count Data. Output from Shift Register
13	O	$Z2_{DATA}$	Channel 2 Zero data. Initially low, will go high on rising edge of $Z2_{IN}$, and remain high until a rising edge on $Z2_{RST.}$
21	-	V_{CCINT}	+5V
23	-	GND	GND
24	I	A_2	Quadrature input A_2 (see pin 35)
25	O	$CNT2_{DN}$	Down count from channel 2 (see pin 43)
26	I	B_2	Quadrature input B_2 (see pin 35)
27	O	$CNT2_{UP}$	Up count from channel 2 (see pin 36)
28	I	$Z2_{IN}$	Zero/Reference mark input. Sets $Z2_{DATA.}$ Also clears internal position counter to 0. $Z2_{IN}$ is asynchronous with respect to any other input signal.
31	-	GND	GND
32	-	V_{CCIO}	+5V/+3.3V - I/O Voltage
35	I	A_1	Quadrature input A_1 A_1 and B_1 (pin 37) accept outputs from a quadrature encoded source, eg optical encoder. A_1 and B_1 are nominally +/- 90 degrees out of phase.
36	O	$CNT1_{UP}$	Channel 1 count up. Will pulse high for one clock cycle whenever the quadrature decoder detects a upwards movement.
37	I	B_1	Quadrature input B1 (see pin 35)
38	-	GND	GND (Reserved)
39	I	Z_{IN} (RST)	Zero/Reference mark input. Reset internal position counter to 0. Sets $Z1_{DATA.}$ $Z1_{IN}$ is asynchronous with respect to any other input signal.
40	I	$\overline{CS}$	Chip Select, when high, CNT_{DATA}, CNT_{UP}, CNT_{DOWN} and Z_{DATA} are undriven (tristate), when low, the pins drive their respective values.
41	-	V_{CCINT}	+5V
43	O	$CNT1_{DN}$	Channel 1 count down. Will pulse high for one clock cycle whenever the quadrature decoder detects a downwards movement.
44	I	CHSLCT	Select source channel for parallel load into shift register. If CHSLCT is low, channel 1 is used, if CHSLCT is high, channel 2 is used.

***All other package pins should be tied to GND to ensure correct operation.**

Functional Block Diagram:



Component Description

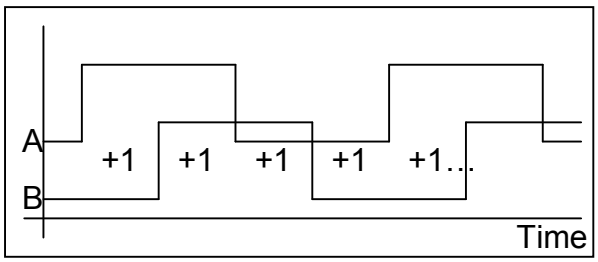
Digital Input Filter

The digital input filter is responsible for removing noise from the incoming quadrature signals. A delay filter of 2 clock cycles rejects spikes of short duration. The input data is tested for a stable level being present for 2 consecutive rising clock edges, and the filtered output will only change after the input signal has remained consistent for this time. Short noise spikes and pulses of less than shorter than 2 clock periods are ignored.

The operation of a digital input filter placesadditional constraints on the maximum speed of input signals A and B. Because the signals must remain constant for 2 clock cycles, they can have an absolute maximum frequency of (CLK_{QD} / 2), and should be slower than this where noise is present. It is recommended that the input frequency is less than CLK_{QD} / 4.

Quadrature Decoder

The quadrature decoders decode the filtered signals into count information. 4X quadrature decoders are implemented, and the counter will increase or decrease by one for each signal transition. (see inset diagram)



The decoder samples the filtered A_1_ and B_1 signals (A_2 and B_2 for channel 2), and calculates the up/down transition based on current and past state. When a transition is detected, either $CNT1_{UP}$ or $CNT1_{DN}$ will go high for one clock cycle ($CNT2_{UP}$ or $CNT2_{DN}$ for channel 2). These pulses also form inputs to the internal counter.

Input line A_1 leading line B_1 results in counting up. Line B_1 leading line A_1 results in counting down. (Similarly for A_2 and B_2)

Illegal state transitions (A_n and B_n both changing between two CLK_{QD} rising edges) will cause the count to remain constant.

Counter

This consists of dual 12 bit binary up/down counters which counts on rising edges of the pulses output from the quadrature decoders.

All 12 bits of data are passed in parallel to the shift register via a multiplexer to select the channel (CHSLCT).

The counter is cleared to 0 asynchronously by a rising edge on $Z_{IN.}$

Shift Register

The Shift Register operates on a separate clock to the rest of the components.

Data is latched into the shift register on a rising edge of CLK_{SR} while PL_{SR} is held high.

The LSB of the counter's value is then available immediately on CNT_{DATA}.

On each further rising edge of CLK_{SR} (with PL_{SR} low) the next highest bit of the counter's value is latched to $CNT_{DATA.}$

After 11 CLK_{SR} rising edges, further CLK_{SR} rising edges will latch 0 to CNT_{DATA}.

At any point if PL_{SR} is held high for one rising edge of CLK_{SR} then a new count value will be latched into the shift register.

Zero/ Reference Mark

Each channel has independent Zero/ Reference Mark logic. The following description is for channel 1, but applies equally to channel 2.

A rising edge on $Z1_{IN}$ will:

- Set the channel 1 counter to have value 0
- Latch $Z1_{DATA}$ high.

$Z1_{DATA}$ will then remain high until a rising edge occurs on $Z1_{RESET}$, which will latch $Z1_{DATA}$ low again.

If a rising edge occurs on $Z1_{IN,}$ while $Z1_{RESET}$ is high, then $Z1_{DATA}$ will still become latched high.

$Z1_{IN}$ and $Z1_{RESET}$ are asynchronous input signals.

Tristate Output

All chip outputs are tristate-capable, to permit easy connection to a bus. When CS is high, all outputs become undriven. When CS is low, outputs drive their respective values.